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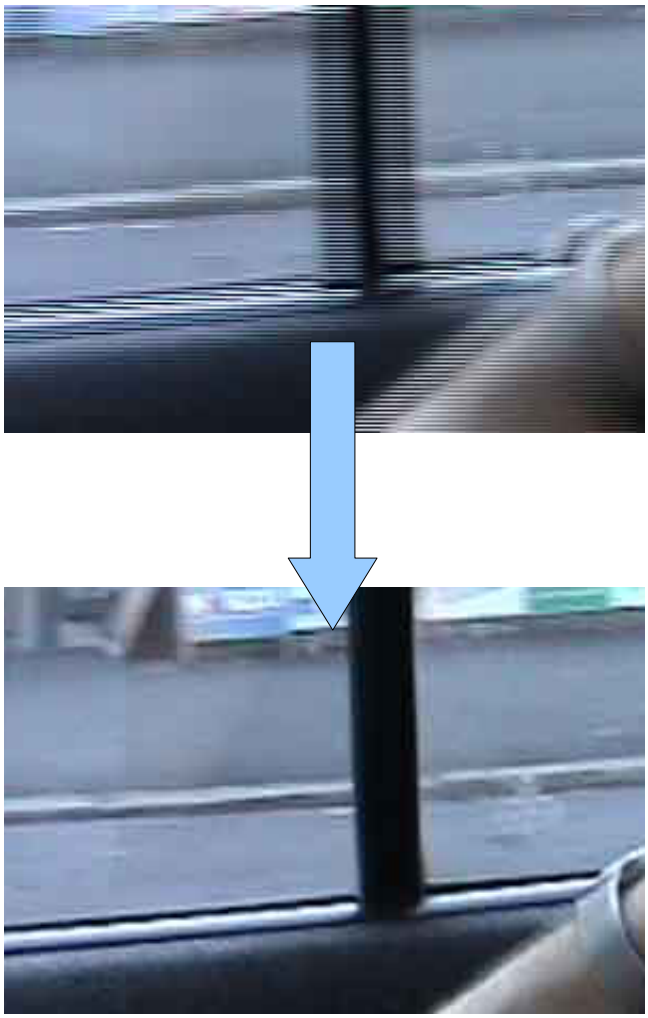
IP datasheet

IV-DEINT
Deinterlacer

Features:

- Line Averaging Mode
- Field Insertion Mode
- Adaptive Deinterlacing Mode
- RGB/YCC Input
- Resolution up to 2048x2048
- 1pixel per clock throughput
- Single Field Memory
- Bandwidth efficient architecture
- Low processing delay



Applications

Industrial

Medical

Automotive

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Overview:

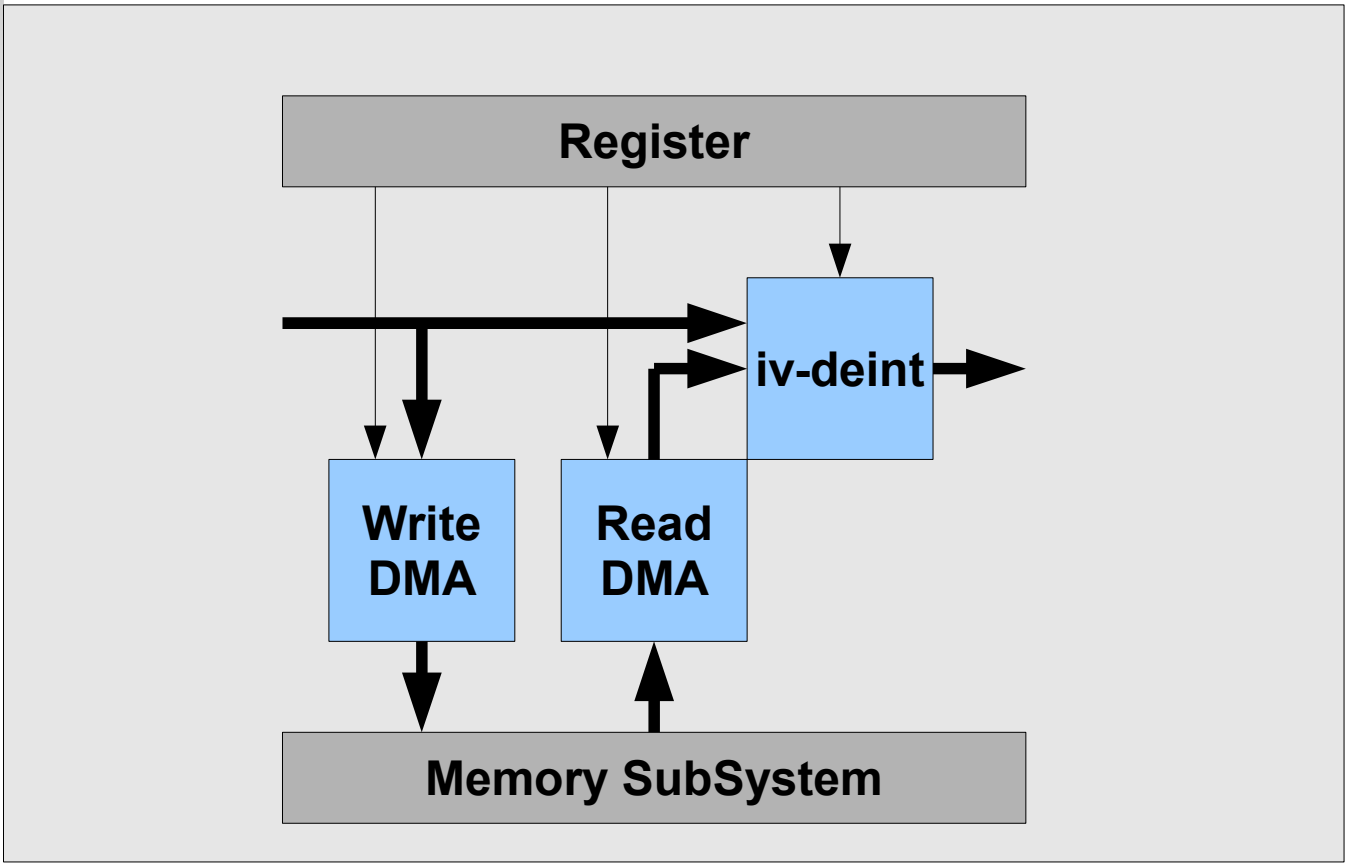
The IV-DEINT IP implements a low delay video deinterlacing algorithm for high resolution images like HD (1920x1080i50/ 1920x1080i60). The maximum resolution is 2048x2048.

The throughput of the design is 1 pixel per cycle on 3 components 8bit each (e.g. RGB or YUV444). The deinterlacer processing delay is about 1 line which makes the IP suitable especially for low latency applications. Line averaging, field insertion and adaptive modes are supported

Programmable parameters are:
- Deinterlacing mode
- Input Video resolution
- Optional DMA setup

Program parameters changes are applied during vertical blanking. The algorithm requires 1 full field storage. Processed pixel are directly displayed.

The design is written in verilog and easily portable to either FPGA or ASIC. It uses generic system interfaces for programming and is delivered with standard video interfaces to be part of a video pipeline. The design can also be packaged with a Write/Read DMA. Programming and DMA interfaces can be easily adapted to any standard like OCP or AHB/AXI.



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