iv-tec

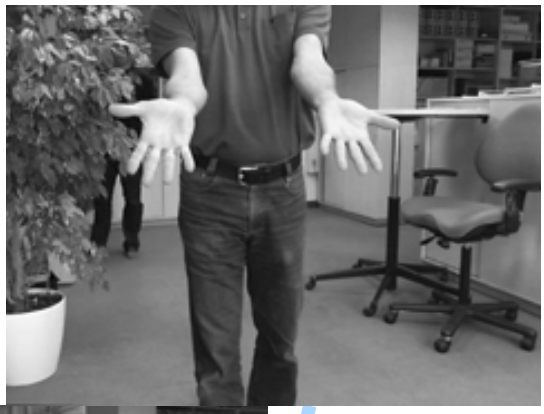
imagination and vision

IP datasheet

IV-CORR
3D Video Processor

Features:

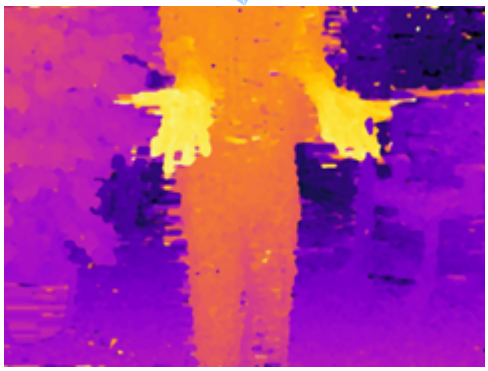
- Stereo Correspondence Calculation
- 64 Disparities
- 75MSampes/sec
- 1 Depth Value per cycle
- Block based matching algorithm



Right Camera

Left Camera

"false color Depth Map



Applications

Industrial

Automotive

Medical

www.iv-tec.com

Overview:

iv-corr implements a 1-dimensional search algorithm for stereo correspondences in stereo pictures.

The algorithms performs a pixel by pixel measurement of the horizontal correlation between pixels in a left and right image. The IP outputs the disparity of the closest match (0-63) and its matching value (actual minimum) for use in subsequent post processing.

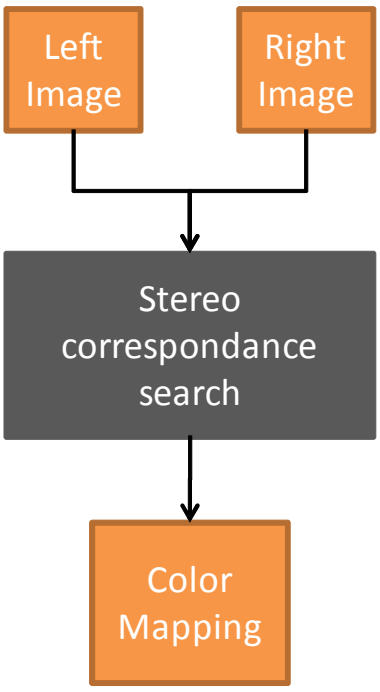
iv-corr operates on pixelrates up to 75Mpixel/sec and with a maximum line size of 1536 pixels.

Programmable Parameters are:

•input picture size

Input pictures to iv-corr have to be rectified (→ iv-rec) to ensure proper results.

The data input to this block are 2 synchronized streaming interfaces (pixel aligned left and right picture)
Program parameters changes are applied during vertical blanking. The algorithm requires no video storage. Processed pixel are directly output for further postprocessing.
The design is written in verilog and easily portable to either FPGA or ASIC. It uses generic system interfaces for programming and is delivered with standard video interfaces to be part of a video pipeline.



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Deliverables

* Verilog 2001 compatible code
* Customized for your application
* Integrated to your existing code
* Easily interfaced to standard I/O standards
* Excellent code and expression coverage
* FPGA proven design
* Real time demos available
* Application support available

HDL Source Licenses

Synthesizable Verilog 2001 RTL*
- (VHDL option available)

Self checking Verilog Testbench **
- VCD dump option
- Expected results generator
- Simulation script

Test stimuli vectors
Test config vectors
- Generic API optional available

Coverage reports
Synthesis script
IP Documentation

* verified tool compatibilities as of today (Modelsim/NCSIM)

Netlist Licenses

For FPGA platforms:
- XILINX
- Lattice
- Altera

For ASIC: please ask

IP Options (please ask)

Interface Adaptations:
Register Interface: OCP Slave/ AHB
DMA Interfaces: OCP Master / AXI

Bundling with other iv-tec IP

iv-tec GmbH
email: info@iv-tec.com

www.iv-tec.com