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IP datasheet

IV-BAYER
Bayer Pattern Interpolator

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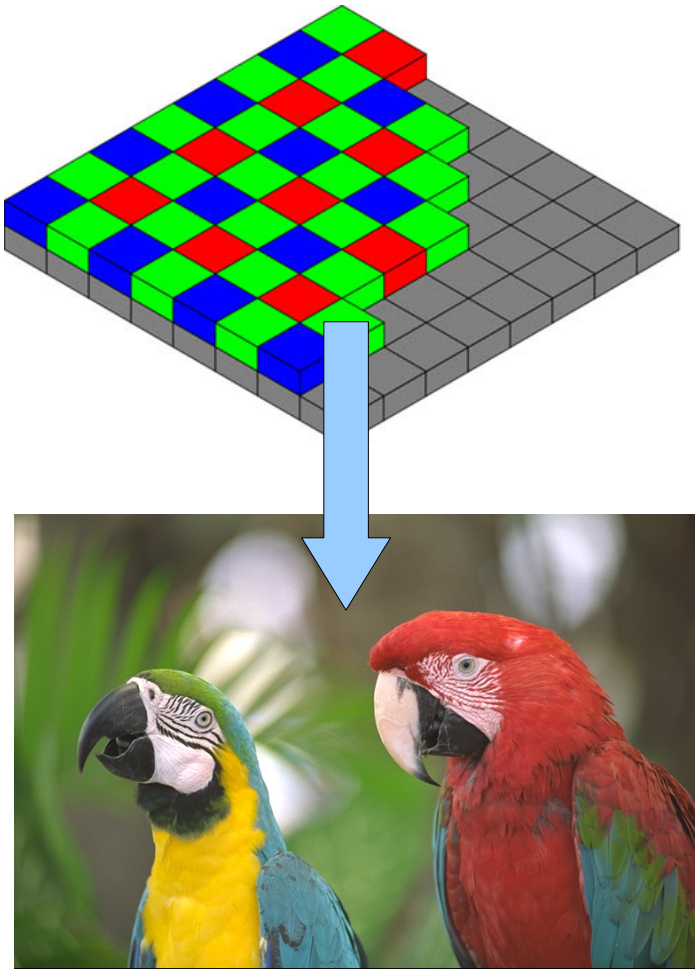

Features:

- Bayer Pattern Input
- RGB Output
- Resolution up to 2048x2048
- 1 pixel per clock throughput
- Low processing delay

Applications

Industrial

Medical

Automotive

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Overview:

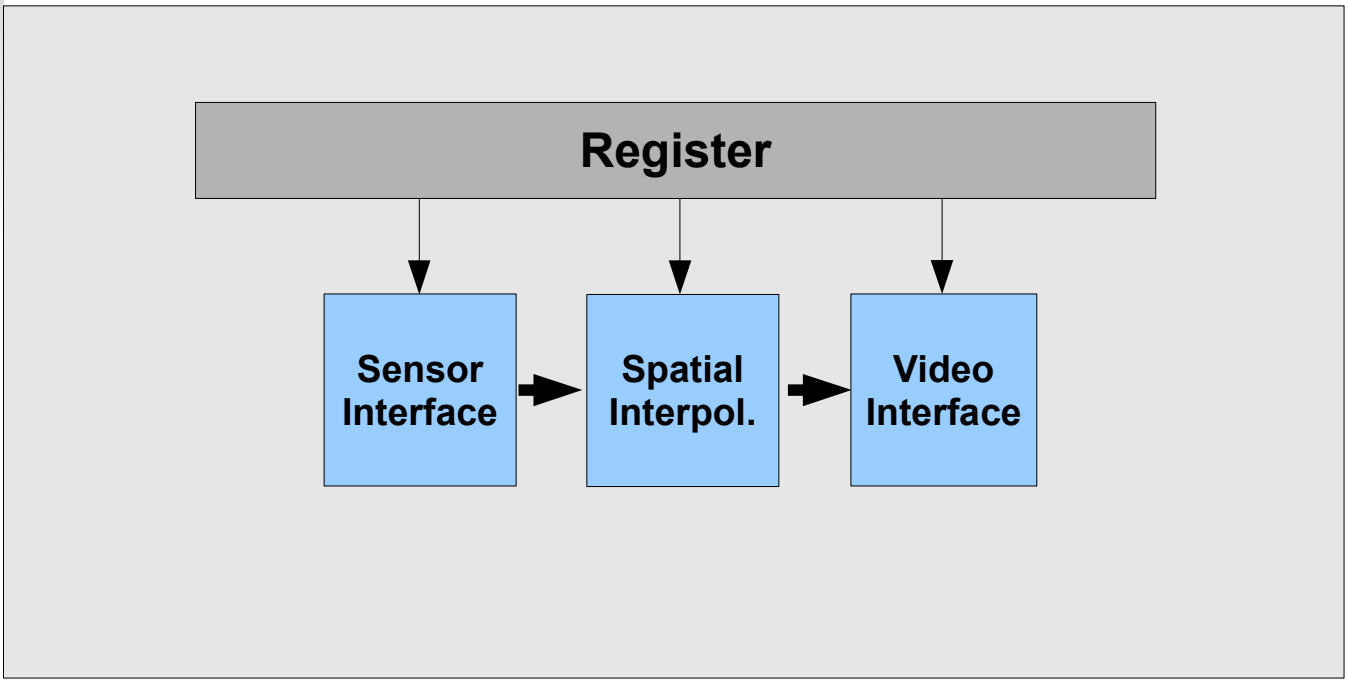
The IV-Bayer IP implements a bayer pattern interpolation algorithm for high resolution image sensors (e.g. 1920x1080). The maximum resolution is 2048x2048.

The throughput of the design is 1 pixel per cycle on 3 components 8bit each (RGB).

Programmable parameters are:
- Bayer Pattern Offset
- Sensor Resolution

Program parameters changes are applied during vertical blanking. Processed pixel are directly displayed.

The design is written in verilog and easily portable to either FPGA or ASIC. It uses generic system interfaces for programming and is delivered with standard video interfaces to be part of a video pipeline. The design can also be packaged with a Write DMA. Programming and DMA interfaces can be easily adapted to any standard like OCP or AHB/AXI.



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Deliverables

* Verilog 2001 compatible code
* Customized for your application
* Integrated to your existing code
* Easily interfaced to standard I/O standards
* Excellent code and expression coverage
* FPGA proven design
* Real time demos available
* Application support available

HDL Source Licenses

Synthesizable Verilog 2001 RTL*
- (VHDL option available)

Self checking Verilog Testbench **
- VCD dump option
- Expected results generator
- Simulation script

Test stimuli vectors
Test config vectors
- Generic API optional available

Coverage reports
Synthesis script
IP Documentation

Netlist Licenses

For FPGA platforms:
- XILINX
- Lattice
- Altera

For ASIC: please ask

IP Options (please ask)

Interface Adaptations:
Register Interface: OCP Slave/ AHB

* verified tool compatibilities as of today (Modelsim/NCSIM)

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